

Refine Search

Search Results -

Terms	Documents
L8 same L7	24

Database:

US Pre-Grant Publication Full-Text Database
 US Patents Full-Text Database
 US OCR Full-Text Database
 EPO Abstracts Database
 JPO Abstracts Database
 Derwent World Patents Index
 IBM Technical Disclosure Bulletins

Search:

L9

Search History

DATE: Sunday, September 17, 2006 [Purge Queries](#) [Printable Copy](#) [Create Case](#)

<u>Set Name</u> side by side	<u>Query</u>	<u>Hit Count</u>	<u>Set Name</u> result set
<i>DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR</i>			
<u>L9</u>	L8 same l7	24	<u>L9</u>
<u>L8</u>	test adj1 circuit	25494	<u>L8</u>
<u>L7</u>	match adj2 circuit	5911	<u>L7</u>
<u>L6</u>	L5 same l2	0	<u>L6</u>
<u>L5</u>	variable near3 (load or resistor)	93159	<u>L5</u>
<u>L4</u>	l2 same test\$	17	<u>L4</u>
<u>L3</u>	L2 same load	8	<u>L3</u>
<u>L2</u>	match adj1 detection adj1 circuit	202	<u>L2</u>
<i>DB=USPT; PLUR=YES; OP=OR</i>			
<u>L1</u>	6697277[pn]	1	<u>L1</u>

END OF SEARCH HISTORY

[First Hit](#) [Previous Doc](#) [Next Doc](#) [Go to Doc#](#)

End of Result Set

☐ [Generate Collection](#) [Print](#)

L11: Entry 4 of 4

File: DWPI

Jan 27, 2005

DERWENT-ACC-NO: 2005-150714

DERWENT-WEEK: 200516

COPYRIGHT 2006 DERWENT INFORMATION LTD

TITLE: Test circuit for content addressable memory match detection circuit, has test line that is switchably coupled to line of match detection circuit to provide load on line and to test feature of match detection circuit

Basic Abstract Text (6):

ADVANTAGE - The test line is switchably coupled to a line of the detection circuit to provide the load on the line and to test the feature of the detection circuit, thus effectively and reliably determining a margin of the match detection circuit.

[Previous Doc](#) [Next Doc](#) [Go to Doc#](#)

[First Hit](#) [Fwd Refs](#)[Previous Doc](#)[Next Doc](#)[Go to Doc#](#)

Generate Collection

Print

L9: Entry 6 of 24

File: USPT

Feb 24, 2004

DOCUMENT-IDENTIFIER: US 6697277 B2

TITLE: Content addressable memory (CAM) having a match line circuit with selectively adjustable pull-up impedances

Detailed Description Text (16):

Accordingly, FIG. 5 illustrates a reference circuit 500 which features devices substantially similar to those included within circuit 300, and which are preferably formed upon the same chip as circuit 300 and the CAM array. However, in contrast to a plurality of circuits 300 associated with the CAM array cells, there need only be a single reference circuit 500. In effect, reference circuit 500 is used as a "dummy" or test circuit which is self-adjusting so as to determine a desired impedance strength for the pull-up devices included in the actual operating match line circuits 300.

[Previous Doc](#)[Next Doc](#)[Go to Doc#](#)

[First Hit](#) [Fwd Refs](#)[Previous Doc](#)[Next Doc](#)[Go to Doc#](#)

Generate Collection

Print

L9: Entry 8 of 24

File: USPT

Sep 9, 2003

DOCUMENT-IDENTIFIER: US 6618279 B2

TITLE: Method and apparatus for adjusting control circuit pull-up margin for content addressable memory (CAM)

Detailed Description Text (16):

Accordingly, FIG. 5 illustrates a reference circuit 500 which features devices substantially similar to those included within circuit 300, and which are preferably formed upon the same chip as circuit 300 and the CAM array. However, in contrast to a plurality of circuits 300 associated with the CAM array cells, there need only be a single reference circuit 500. In effect, reference circuit 500 is used as a "dummy" or test circuit which is self-adjusting so as to determine a desired impedance strength for the pull-up devices included in the actual operating match line circuits 300.

[Previous Doc](#)[Next Doc](#)[Go to Doc#](#)